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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,044	12/04/2001	Gilbert C. Sih	010264	9617

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Qualcomm Incorporated
Patents Department
5775 Morehouse Drive
San Diego, CA 92121-1714

EXAMINER	
NGUYEN, HAU H	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,044	SIH ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen .	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/27/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-5, 9-11, 13-14, 31-33, 35-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Kohashi et al. (European Patent No. 1,146,746).

Referring to claims 1-2, 4-5, 9-11, 13-14, 31-33, 35-36, as shown Fig. 8, Kohashi et al. teach a video processing apparatus including a video input/output unit 800 which inputs/outputs an input video or a display video, an external memory 802 (a source memory) which stores video data or coded data, an encoding/decoding unit 803 which performs an encoding/decoding processing to the video data or the coded data, and a DMA bus which performs the data transmission between the video input/output unit 800 or the encoding/decoding unit 803 and the external memory 802 (a VDMA). The encoding/decoding unit 803 comprises: a data processing unit 804 encodes or decodes video data; an internal memory 805 (a destination memory) stores the video data read out (copied from) from the external memory 802 (a source memory); a control unit 806 outputting a content of a processing and the processing timing to the data processing unit 804 and, further outputting a start address of the data region which is transmitted from the internal memory 805 to the data processing unit 804 to the internal memory control unit 807. The internal memory control unit 807 comprises a two dimensional address generating unit 808 for generating addresses according to the setting information from the control unit 806 and

an address conversion unit 809 for converting an address input from the two dimensional address generating unit 808 into an access address to the internal memory 805 (command specifying a multi-dimensional block of video data) (see paragraphs 52-55, page 8). As shown in Fig. 10, Kohashi et al. teach a diagram for explaining the correspondence between a (two dimensional) logical address and a (one dimension) physical address (linearly addressable storage units) of the rectangular region (horizontal 48 pixels X vertical 48 pixels) (specifying the number of rows and the number of columns) in the internal memory 805 (paragraphs 58, page 9). The generation of source addresses including specifying a start address to access the external memory (source memory), and generation of destination addresses including specifying a start address to access the internal memory (destination memory) is described in paragraphs 64-65, pages 9-10 with reference to Fig. 10.

Referring to claims 17 and 19, as cited above, with reference to Fig. 8, Kohashi et al. teach a first memory (external memory 802) (first cache) for storing candidate block to be encoded, and a second memory (an internal memory 805) (second cache) to store a set of video data blocks from which to encode the candidate video block, and a two dimensional address generating circuit for calculating the difference between the source video block (transmitted from the external memory) and the destination video block (in the internal memory).

In regard to claim 21-24, as also cited above, Kohashi et al. teach a VDMA controller for performing copying blocks of video data from the external memory to the internal memory in response to a DMA command, which specifying the number of rows and number of columns of the block of video data. Also cited above, Kohashi et al. teach the video memory is linearly addressable.

Referring to claim 26, as cited above, Kohashi et al. teach the command specifying a start source address in the first memory, and a start destination address in the second memory.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 6, 12, 25, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohashi et al. (European Patent No. 1,146,746) in view of Langendorf et al. (U.S. Patent No. 6,313,766).

Referring to claims 3, 6, 12, 25, and 27, as cited above, Kohashi et al. teach all the limitations of claims 3, 6, 12, 25, and 27, except for a jump parameter, and the video block fetched from the memory having multiple non-contiguous rows.

However, Langendorf et al. teach a system, as shown in Fig. 5, comprising, a processor 510, a system memory 520, a Direct Memory Access (DMA) device 530, and a system bus 515, wherein the memory device 520 includes a source region 524, a destination region 526, and a run/level table 528. The DMA device 530 receiving an input from a (video) source 531 delivers a bit stream 533 of variable length encoded information to the source region 524 in the system memory 520 (a VDMA). With reference to Fig. 7, Langendorf et al. teach the system includes a data structure initialization/copy device 740 includes a memory access engine 742, a start/destination address register 743, a data structure size register 744, a pattern register 745, and

a source address register 746 (col. 5, lines 60-64), wherein, for copy operations, the source region 722 of memory to be copied from is defined by the address stored in the source address register 746 and further defined by the size value stored in the data structure size register 744. The destination region 724 to be copied to is defined by the address stored in the start/destination address register 743 and is again further defined by the size stored in the data structure size register 744 (col. 6, lines 58-67). Langendorf et al. further teach the memory access engine 542 is preferably able to perform scatter-gather type direct memory accesses. Furthermore, as a result of page based memory management schemes of many operating systems, the stream of data may be stored in non-sequential pages of physical memory (block data of non-contiguous rows) (col. 4, lines 60-67, and col. 5, lines 1-5).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Langendorf et al. in combination with the method as taught by Kohashi et al. in order to communicate the physical memory locations of a large block of data (col. 5, lines 2-5).

5. Claims 7-8, 18, 20, 28-30, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohashi et al. (European Patent No. 1,146,746) in view of Kohn (U.S. Patent No. 6,335,950).

Referring to claims 7-8, 18, 20, 28-30, 37, and 38, as cited above, Kohashi et al. teach all the limitations of claims 7-8, 28-30, 37, and 38, except that the system further comprising a processor issuing command to the VDMA via a first bus, and a digital signal processor issue commands to the VDMA via a second bus; and the system further comprising a motion estimation unit.

However, Kohn teaches a dual prime motion estimation based on an average of previous field references in a flexible, yet high performance manner. The apparatus has a command memory for storing a motion estimation command list segment, which in turn contains a search command for specifying a merged search operation over one or more search positions (col. 3, lines 1-5). As shown in Fig. 1, Kohn teaches a system for processing and encoding video data comprising a processor 102, a video DSP 104, and a motion estimation engine 100, and further teaches the video DSP 104 works in parallel with the processor 102 to off-load compute intensive pixel level processing operations. Internally, the video DSP 104 contains a separate DMA processor (a video DMA) and a DSP processor connected by a double buffered working memory. The DMA processor transfers data to and from the external SDRAM 200 while the DSP processor performs signal processing operation (which implied that the DMA processor communicates with the DSP processor via a bus (second bus) different from the first bus (bus 103 and 105), which communicates between the DSP processor and the processor 102 (col. 5, lines 8-16). Fig. 2 shows the details of the motion estimation 100, which comprises an internal cache 212-215, a differential calculator 216 for calculating distortion metrics between blocks of video data (see also to Fig. 4, and col. 6, lines 44-51). Kohn further teaches the memories 214 and 215 can stores a complete frame (col. 6, lines 8-12).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Kohn in combination with the method as taught by Kohashi et al. in order to obtain faster search operation (col. 3, lines 66-67, and col. 4, lines 1- 12).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

03/04/2005

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
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